SERVICE MANUAL
& PARTS LIST

(without price)

ELECTRONIC KEYBOARD

HT-3000

JAN. 1987

HT-3000

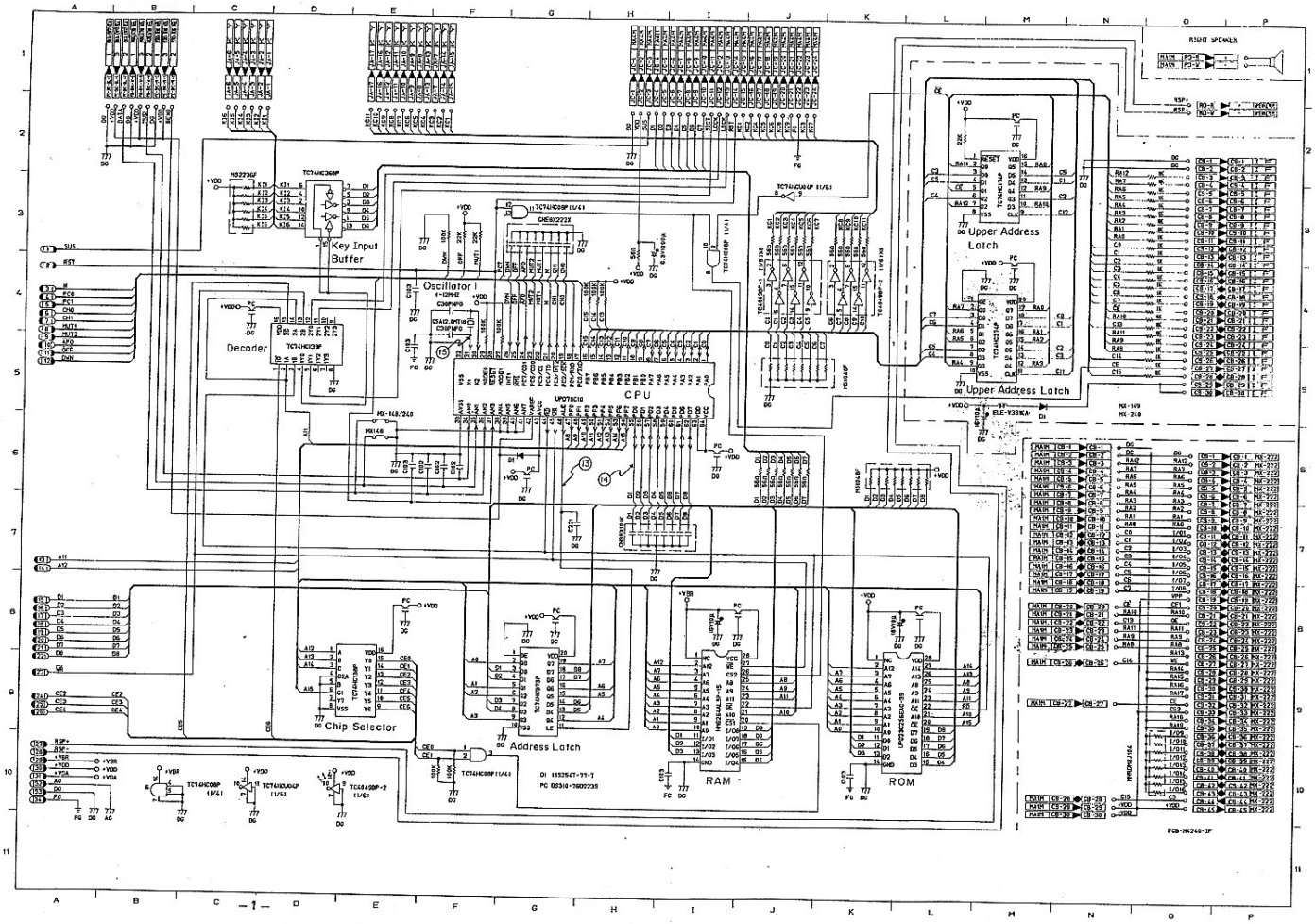
CASIO

CASIO COMPUTER CO., LTD.

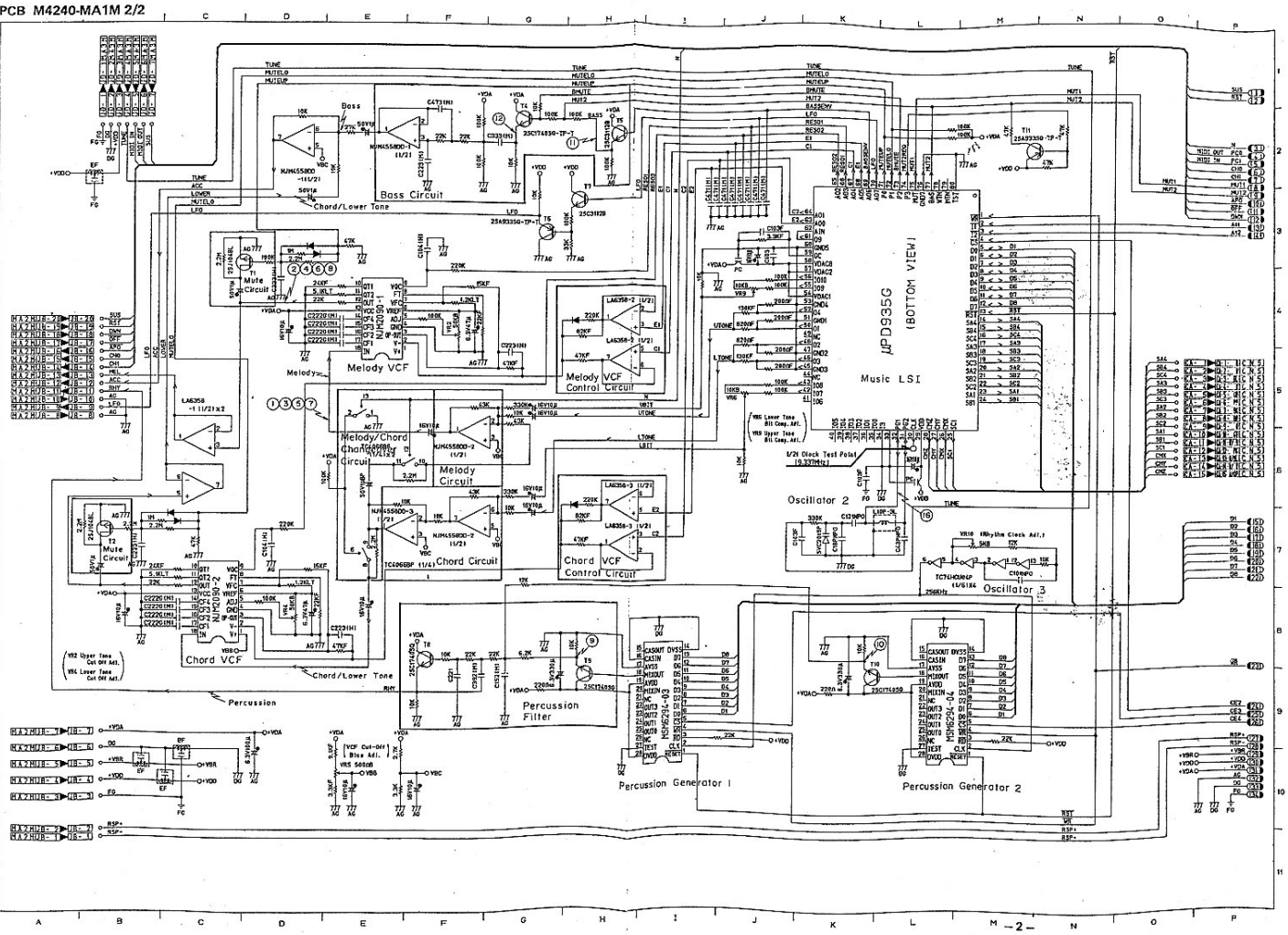
PRINTED IN JAPAN

1. SCHEMATIC DIAGRAM

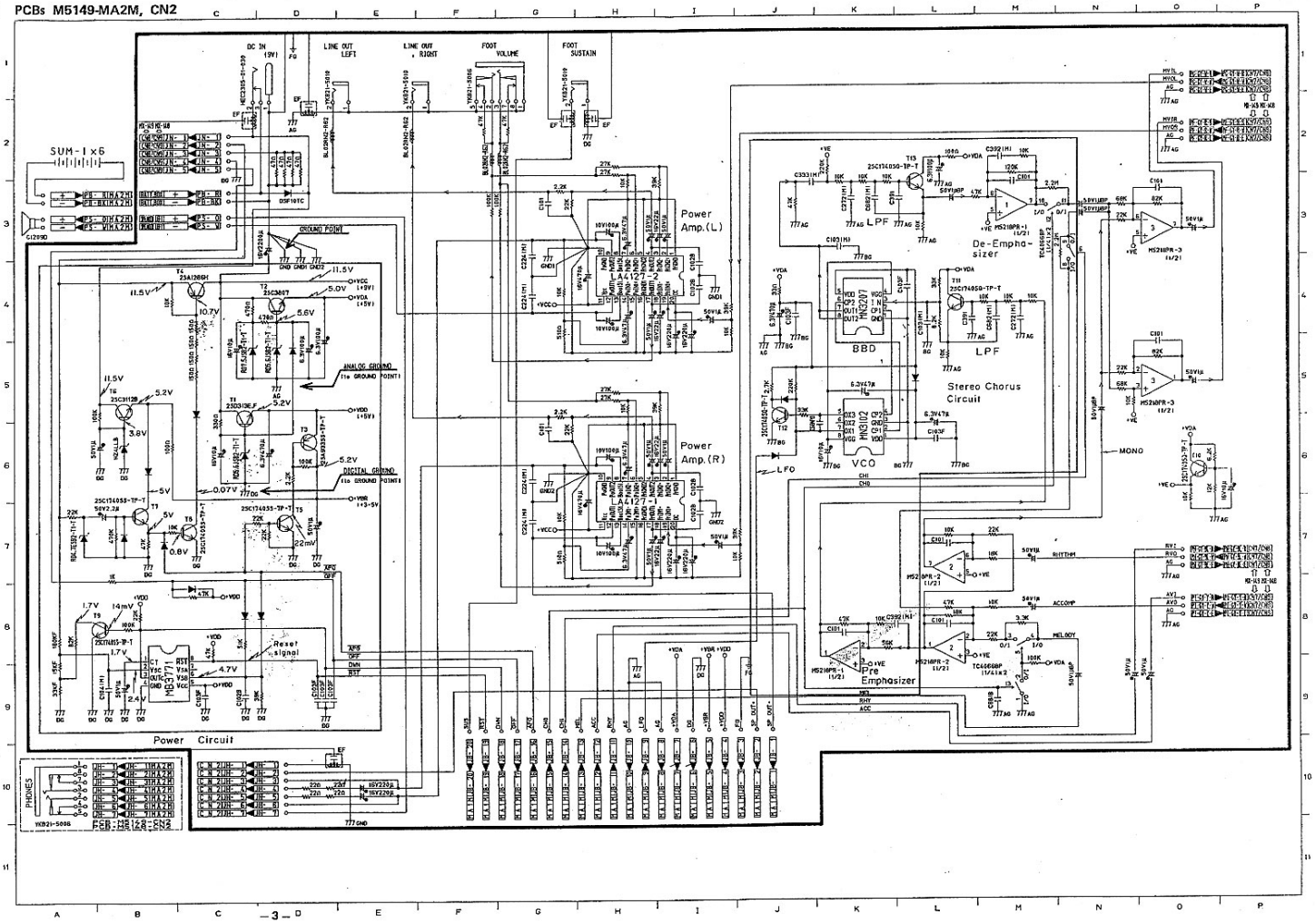
1-1. PCBs M4240-MA1M 1/2, M4240-IF

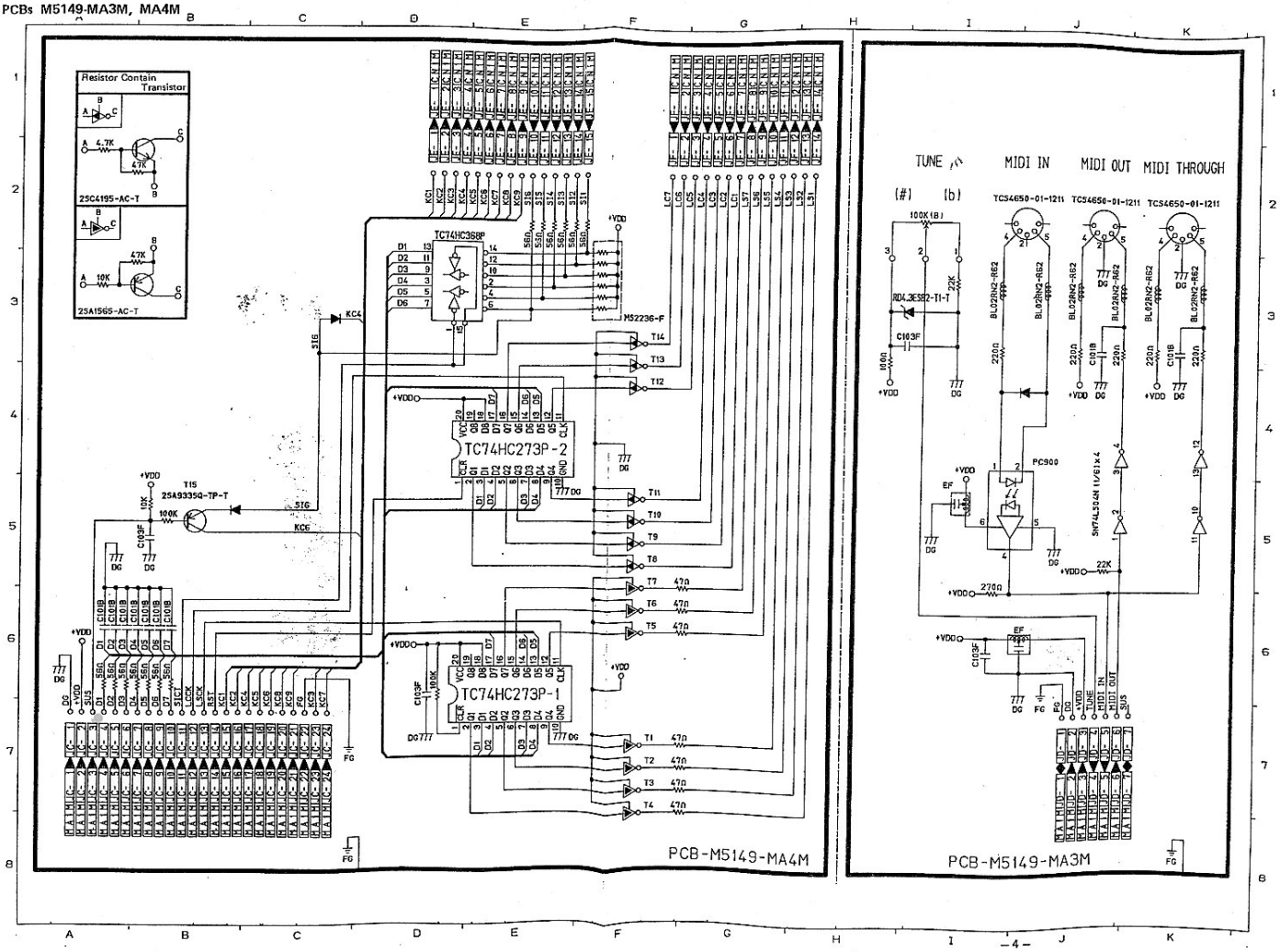


1-2. PCB M4240-MA1M 2/2

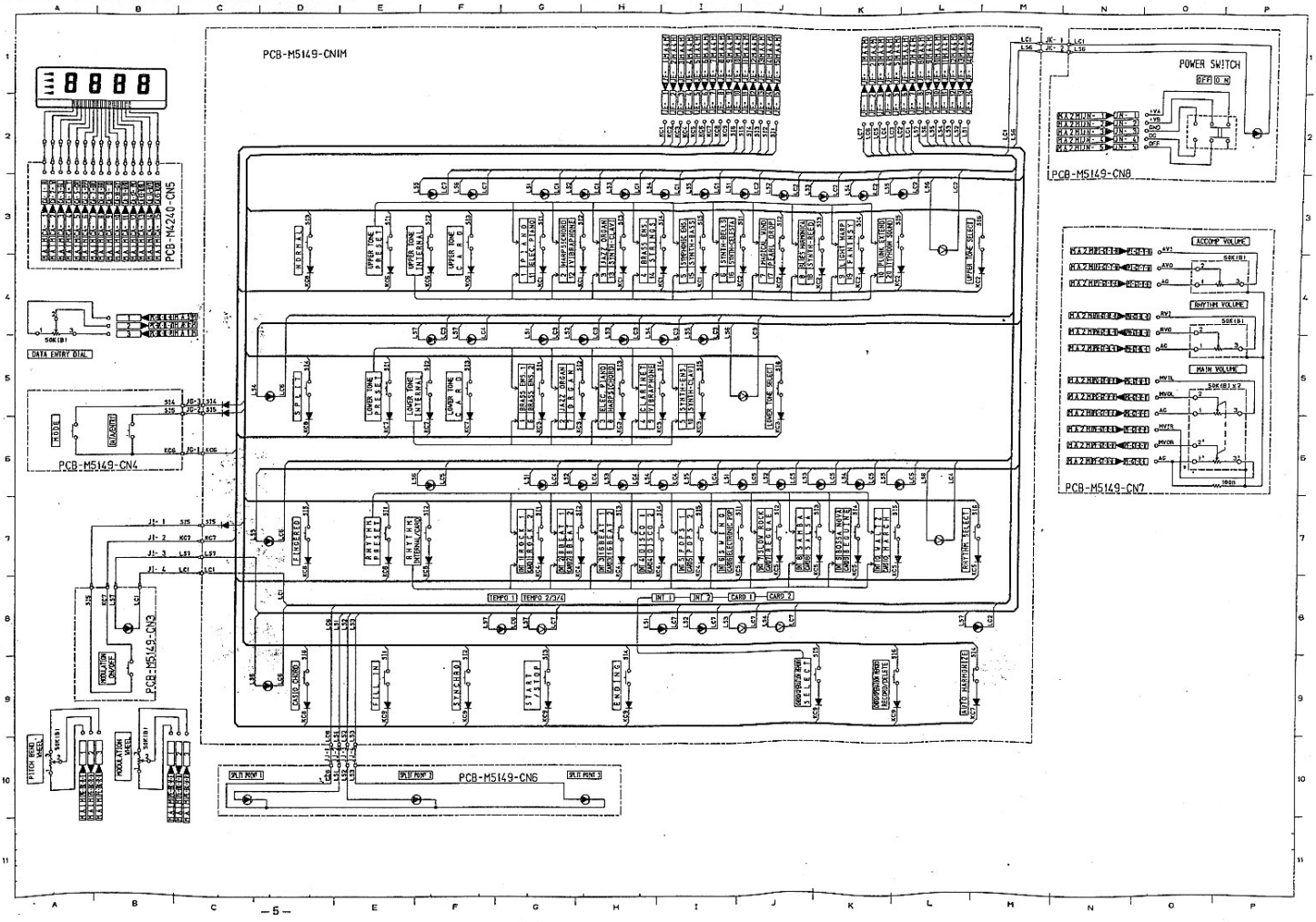


1-3. PCBs M5149-MA2M, CN2

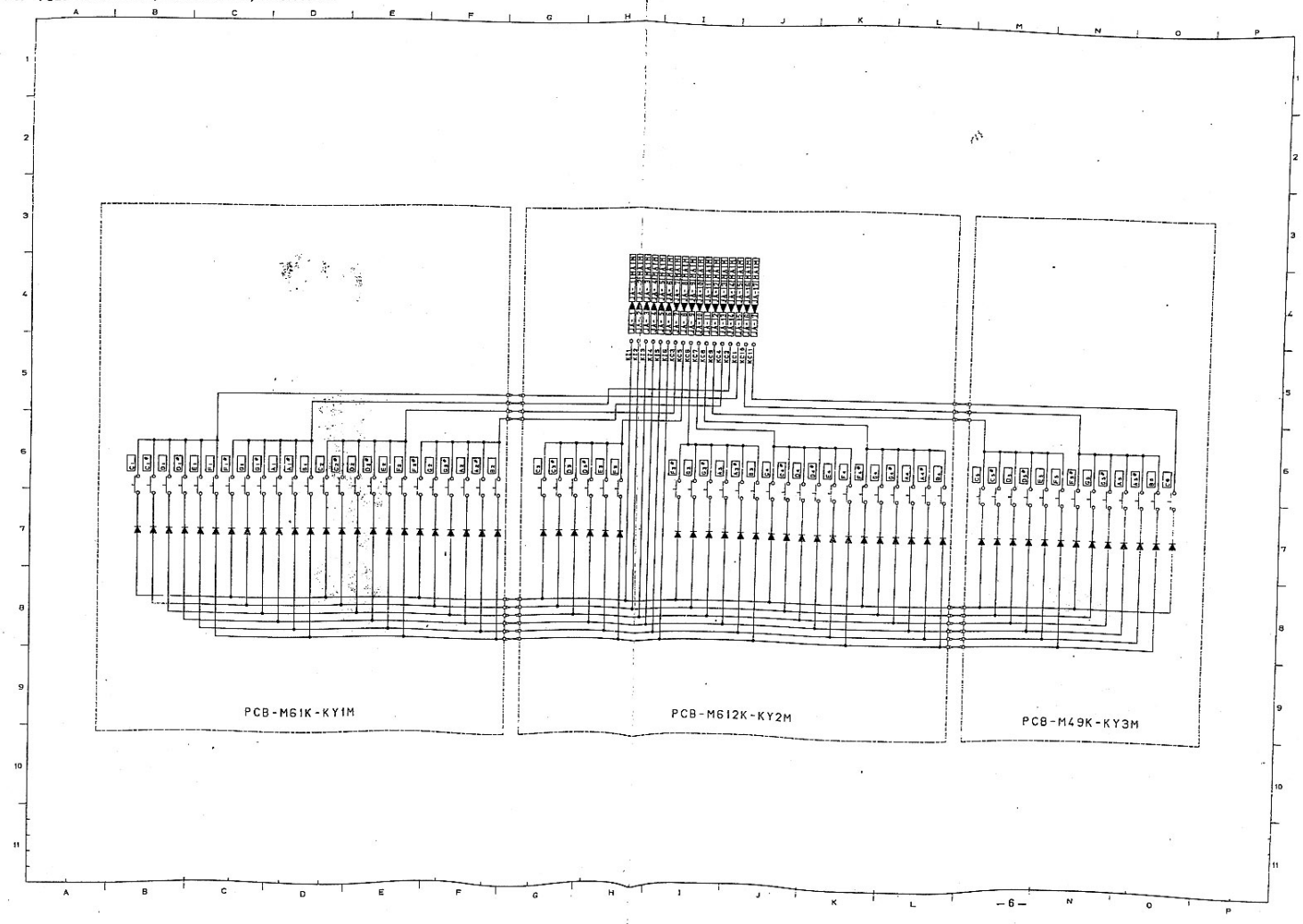




1-5. PCBs M5149-CN1, CN3, CN4, CN6, CN7, CN8, M5240-CN5

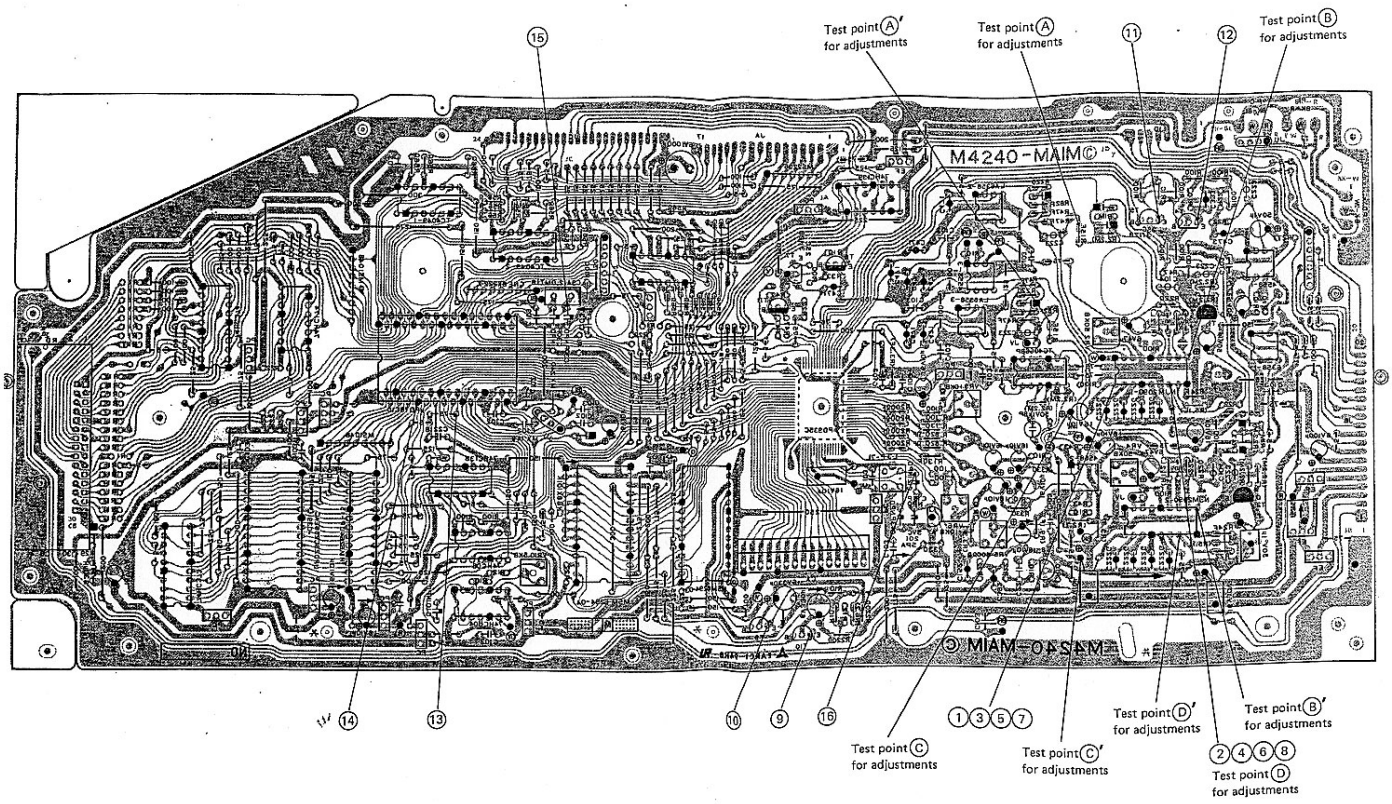


1-6. PCBs M61K-KY1M, M612K-KY2M, M49K-KY3M

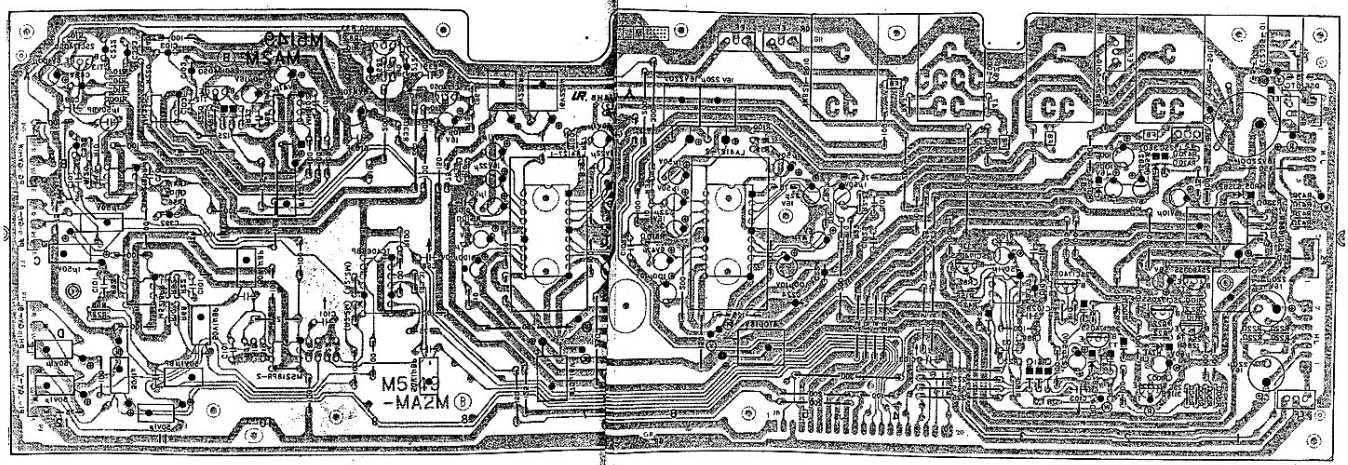


2. PCB VIEW

2-1. PCB M4240-MA1M



2-2. PCB M4240-MA2M



3. MAJOR WAVEFORMS

Notes: (1) Waveforms ① ~ ⑥ are observed by varing DATA value in MODE 10 (Cutoff Frequency) of preset tone No.17 (Pearl Drop)

(2) Oscilloscope screen readings

Channel 1 (Upper Waveform) P10x 0.2V

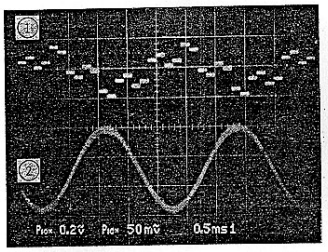
Channel 2 (Lower Waveform) P10x 50mV

Sweep Time 0.5 ms

Probe attenuation 10 : 1

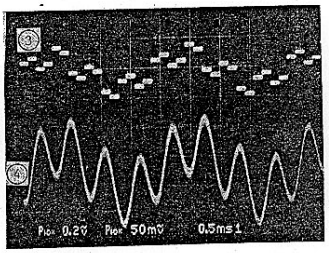
AC range

Triggering Channel



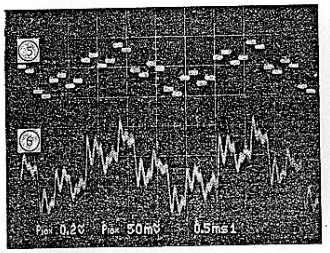
① NJM2091-1 pin 18
② NJM2090-1 pin 12

Tone: Pearl Drop
MODE 10, DATA 8



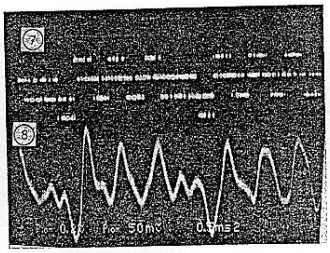
③ NJM2090-1 pin 18
④ NJM2090-1 pin 12

Tone: Pearl Drop
MODE 10, DATA 18 (preset DATA)



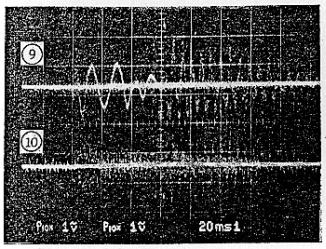
⑤ NJM2090-1 pin 18
⑥ NJM2090-1 pin 12

Tone: Pearl Drop
MODE 10, DATA 26

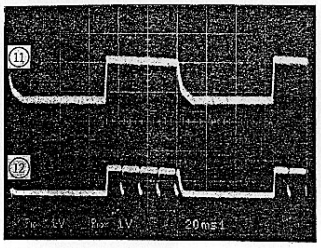


⑦ NJM2090-1 pin 18
⑧ NJM2090-1 pin 12

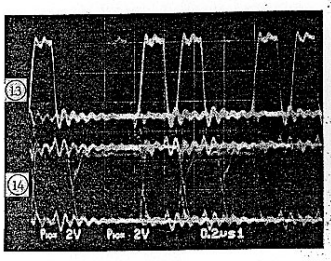
Tone: Pearl Drop
MODE 10, DATA 31, MODE 10, DATA 16



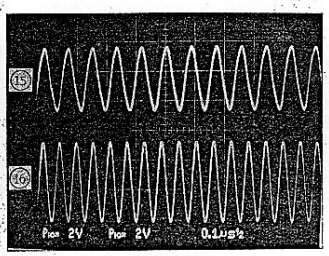
⑨ Percussion signal T9 Emitter
⑩ Percussion signal T10 Emitter



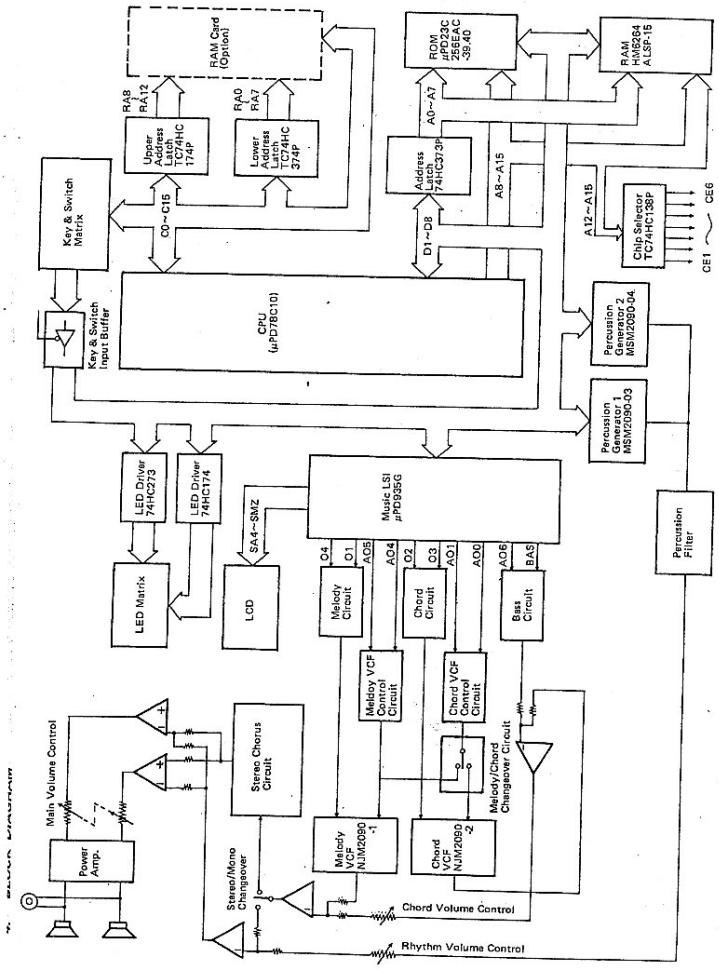
⑪ Bass envelope T5 Emitter
⑫ Bass signal T4 Emitter



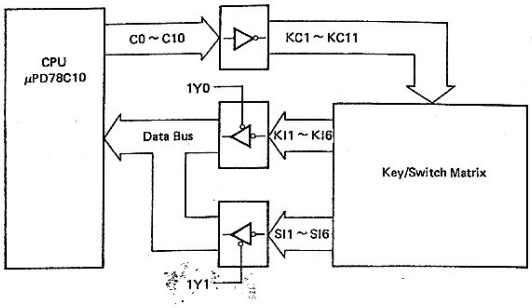
⑬ Signal ALE μPD78C10 pin 46
⑭ Data Bus (D1) μPD78C10 pin 55



⑮ Clock pulse μPD78C10 pin 31
⑯ Clock pulse μPD935 pin 32



5. KEY & SWITCH MATRIX



The CPU outputs signals C0 ~ C10 which become key common signals KC1 ~ KC11 and periodically provides signals 1Y0 and 1Y1 via LED controller to read key and switch input informations.
The following table shows the key matrix.

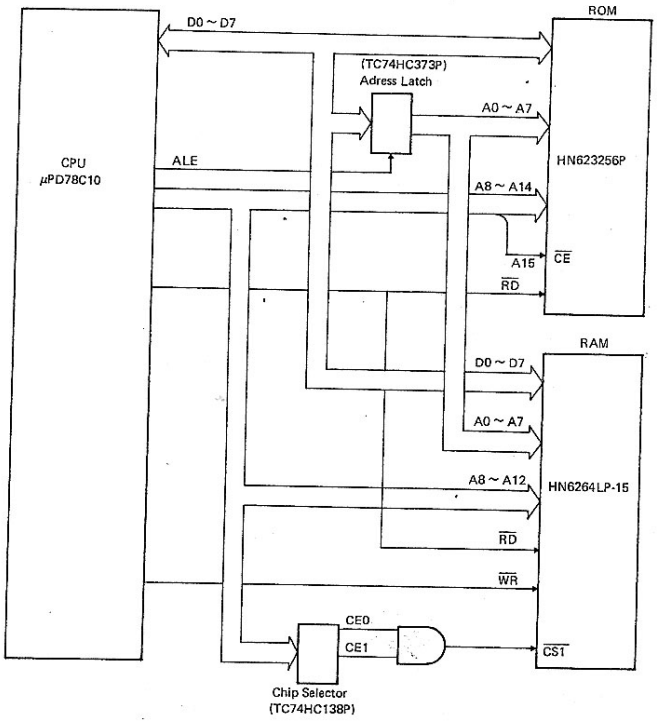
	KC1	KC2	KC3	KC4	KC5	KC6	KC7	KC8	KC9	KC10	KC11
KI1	C1	F#1	C2	F#2	C3	F#3	C4	F#4	C5	F#5	C6
KI2	C#1	G1	C#2	G2	C#3	G3	C#4	G4	C#5	G5	
KI3	D1	G#1	D2	G#2	D3	G#3	D4	G#4	D5	G#5	
KI4	D#1	A1	D#2	A2	D#3	A3	D#4	A4	D#5	A5	
KI5	E1	A#1	E2	A#2	E3	A#3	E4	A#4	E5	A#5	
KI6	F1	B1	F2	B2	F3	B3	F4	B4	F5	B5	
SI1	Upper PIANO	Upper SYNTH. BELLS	Lower BRASS ENS.	ROCK 1	SWING 1	Upper PRESET	Lower PRESET	Rhythm PRESET	FILL IN		
SI2	Upper ELEC. PIANO	Upper MAGICAL WIND	Lower JAZZ ORGAN	8 BEAT	SLOW ROCK	Upper INTERNAL	Lower INTERNAL	Rhythm INTERNAL /CARD	SYNCHRO		
SI3	Upper JAZZ ORGAN	Upper BLUES HARMONICA	Lower ELEC. PIANO	16 BEAT 1	SAMBA	Upper CARD	Lower CARD	NORMAL	START/ STOP		
SI4	Upper BRASS ENS.	Upper LIGHT HARP	Lower CLARINET	DISCO 1	BOSSA NOVA	MODE	AUTO HARMO-NIZE	SPLIT	INTRO/ ENDING		
SI5	Upper SYMPHONIC ENS.	Upper PLUNK EXTEND	Lower SYNTH. ENS.	POPS 1	WALTZ	DATA/ ENTRY	MODURA-TION ON/OFF	FINGERED	SONG MEMORY SELECT		
SI6		Upper SELECT	Lower SELECT		Rhythm SELECT			CASIO CHORD	SONG MEMORY RECORD		

6. CPU (μPD78C10) PIN FUNCTION

Pin No.	Signal	In/Out	Function
1 ~ 13	C0~C12	In	Key common signals, LED drive signals, data and address bus for RAM card
14	C13	Out	Output Enable signal. While LOW, the RAM card is able to output data.
15	C14	Out	Write Enable signal. While LOW, the CPU is able to write data in RAM card.
16	C15	Out	RAM card detection signal. The terminal receives LOW level only when a RAM card is inserted.
17	PC0	Out	MIDI data output
18	PC1	In	MIDI data input
19, 20	CH0, CH1	Out	Stereo chorus effect control signals. Stereo Chorus Effect / CH0 / CH1 OFF / LOW / LOW Deep / HIGH / HIGH Shallow / HIGH / LOW
21	N	Out	Melody/Accomp changeover signal. Music LSI μPD935G provides two 4-note polyphonic outputs. The upper 4-note is always for melody while the lower 4-note is for either chord, lower tone or melody in accordance with CASIO CHORD or SPLIT switches statuses. Signal N changes the signal route of the lower 4-note sound either to Melody VCF or Accomp VCF. When signal N is HIGH, the lower 4-note sound signal is provided to Melody VCF whereas being LOW of the signal sends the lower tone to Accomp VCF.
22	MUT 1	In	Melody VCF mute request input. When Music LSI does not generate melody, it sends mute request signal to CPU through this terminal. CPU then provides melody mute command to Music LSI via data bus.
23	MUT 2	In	Chord/Lower tone mute request input. When Music LSI does not provide chord or lower tone, it sends mute request signal to CPU through this terminal. CPU then provides chord or lower tone mute command via data bus.
24	APO	Out	Auto Power Off control signal. When the keyboard is left unoperated for six minutes, the signal falls to LOW shutting the voltages down.
25	OFF	In	The terminal receives LOW when power switch is turned off. CPU then performs the power off transaction.
26	DWN	In	Voltage down signal. Normally LOW level. When the power voltage or VDD (+5V) is too low, the terminal receives HIGH signal, CPU then provides signal APO to shut the voltages down.
28	$\overline{\text{RESET}}$	In	When the power switch is turned on, the terminal receives LOW signal for approximately 100 milliseconds during which the internal circuits of the LSI is reset.
30, 31	X2, X1	In/Out	12MHz clock pulse input/output
32	VSS	–	Ground source

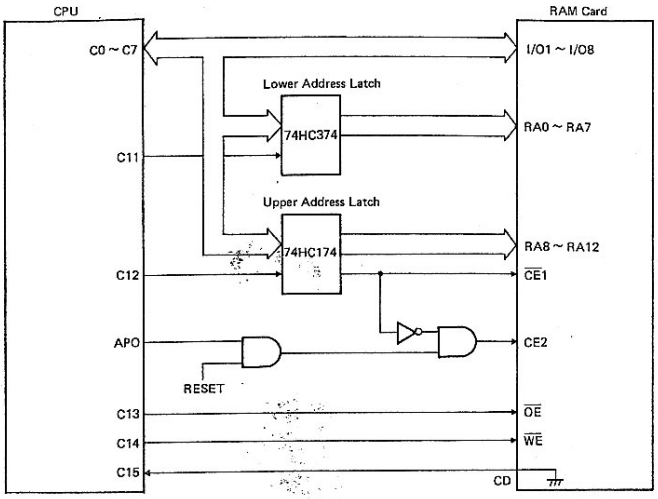
33	AVSS	–	Ground source for the built-in ADCs (Analog to Digital Converter)
34	AN0	In	ADC input from the pitch bender. The voltage level from the pitch bender wheel is transformed in digital signals in a built-in ADC.
35	AN1	In	ADC input from Modulation wheel.
36	AN2	In	ADC input from the entry dial
37	AN3	In	Voltage down detection signal input. When the power voltage is low, the terminal detects it and the CPU flashes the pilot lamp.
42	VAREF	–	Reference voltage for the built-in ADCs
43	AVDD	–	+5V source for the built-in ADCs
44	$\overline{RD}$	Out	Read signal: CPU falls this terminal when it reads data from ROM or RAM.
45	$\overline{WR}$	Out	Write signal. CPU falls this terminal when it writes data in RAM, Music LSI, or Percussion generators.
46	ALE	Out	Address Latch Enable signal. At the rising edge of this signal, the data bus (D0 ~ D7) become the lower address bus (A0 ~ A7).
47~54	A8~A15	Out	Upper address bus
55~62	D0~D7	In/Out	Data bus for ROM, RAM and key matrix. Also control the LEDs driving.

7. ROM & RAM ACCESS



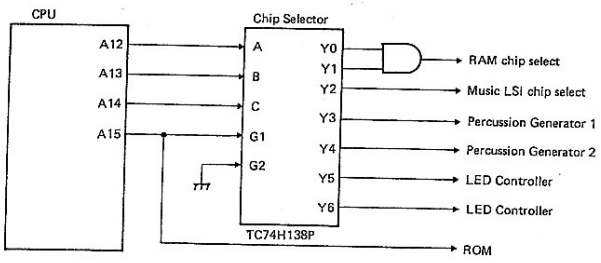
The capacity of the ROM is 32K byte whereas it of the RAM is 8K byte.
The lower address signals A0 ~ A7 are generated from data bus in Address Latch at the rising edge of signal ALE from the CPU.

8. RAM CARD ACCESS



Data signals (I/O1 ~ I/O8) and address signals (RA0 ~ RA12) are provided from CPU terminals C0 ~ C7.
When CPU assigns RAM card address, it first put lower address data on terminals C0 ~ C7 then rise signal C11 to assign the lower address.
Next, the CPU selects the upper address by signals C0 ~ C5 at the rising edge of C12. Chip enable signal $\overline{CE1}$ is generated by being LOW of signal C5 at the rising edge of C12.
The CPU determines RAM card's insertion by receiving LOW at terminal C15.

9. CHIP ENABLING



Each device is selected from CPU by combinations of signals A12 ~ A15.
ROM is assigned directly by signal A15.

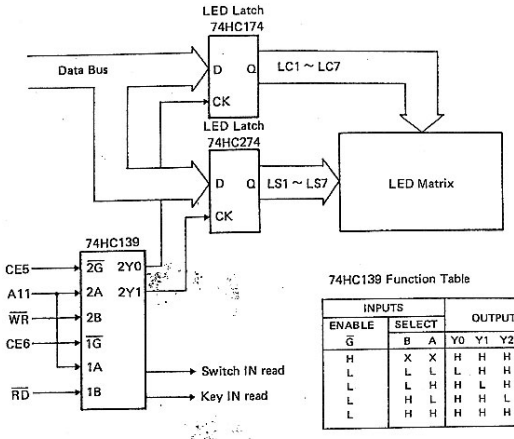
A15	A14	A13	A12	CE	Selected Chip
H	L	L	L	CE0	RAM
H	L	L	H	CE1	
H	L	H	L	CE2	Music LSI
H	L	H	H	CE3	Percussion Generator 1
H	H	L	L	CE4	Percussion Generator 2
H	H	L	H	CE5	LED Controller
H	H	H	L	CE6	
L	–	–	–	–	ROM

'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H= high level, L= low level, X=irrelevant

10. LED DRIVING



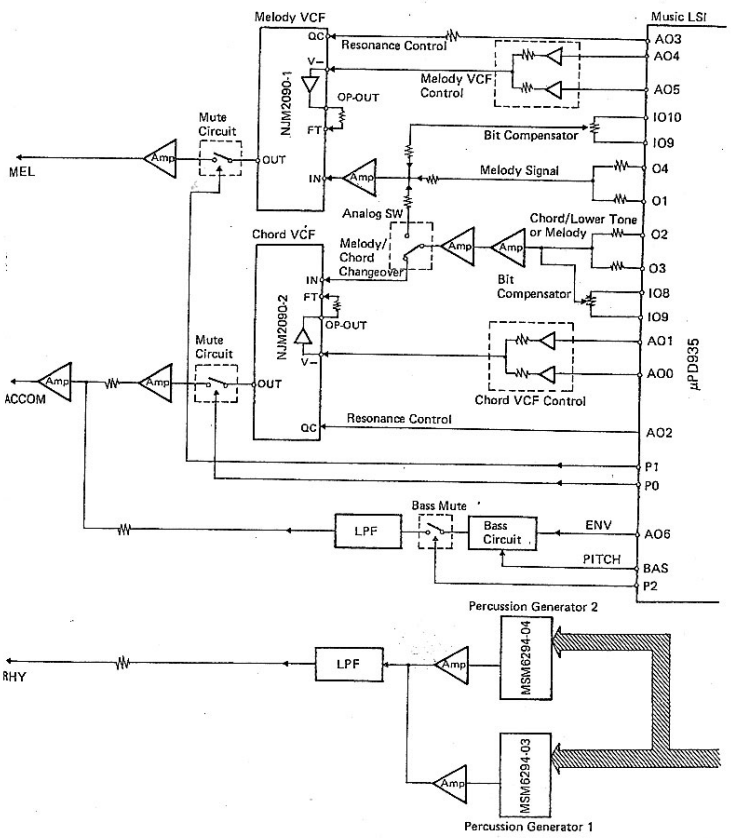
74HC139 Function Table

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

LED Matrix

	LC1	LC2	LC3	LC4	LC5	LC6	LC7
LS1	Upper PIANO	Upper SYNTH. BELLS	Lower BRASS ENS.	ROCK	SWING	SPLIT POINT 1	INT 1
LS2	Upper HARPSI-CHORD	Upper MAGICAL WIND	Lower JAZZ ORGAN	8 BEAT	SLOW ROCK	SPLIT POINT 2	INT 2
LS3	Upper JAZZ ORGAN	Upper BLUES HARMONICA	Lower ELEC. PIANO	16 BEAT	SAMBA	SPLIT POINT 3	CARD 1
LS4	Upper BRASS ENS.	Upper LIGHT HARP	Lower CLARINET	DISCO	BOSSA NOVA	SPLIT	CARD 2
LS5	Upper SYMPHONIC ENS.	Upper PLUNK EXTEND	Lower SYNTH. ENS.	POPS	WALTZ	FING'D	Upper INTERNAL
LS6	POWER	Upper TONE SELECT	Lower TONE SELECT	Rhythm SELECT	Rhythm INTERNAL /CARD	CASIO CHORD	Upper CARD
LS7	Modulation ON/OFF	AUTO HARMONIZE	Lower INTERNAL	Lower CARD		TEMPO (RED)	TEMPO (GREEN)

11. ANALOG CIRCUITS BLOCK DIAGRAM

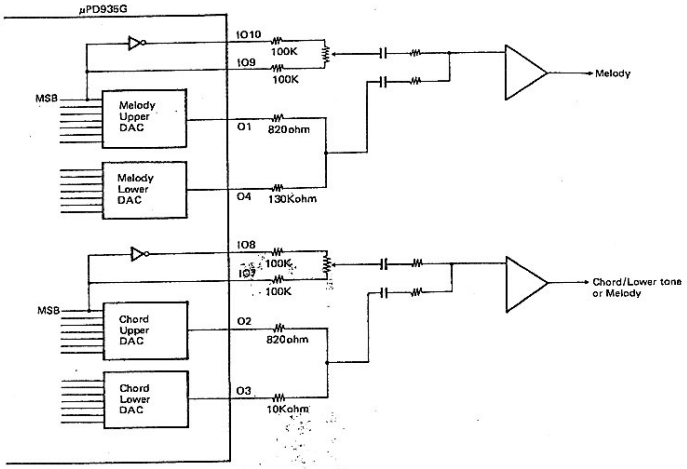


12. MUSIC LSI (μPD935G) PIN FUNCTIONS

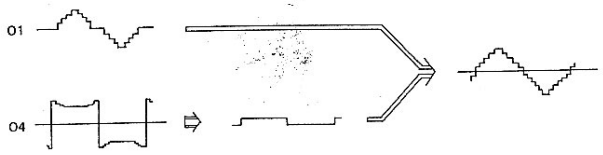
Containing 12 DAC (Digital to Analog Converter)s, the LSI generates melody, bass, chord (lower tone) sounds and VCF control voltages.
μPD935G also drives the LCD.

Pin No.	Terminal	In/Out	Function
1	$\overline{WR}$	In	At the rising edge of this signal, Music LSI receives data or command from the CPU.
2	$\overline{I1}$	In	Receives signal A10 from CPU. When LOW, Music LSI descriminates data bus input as a command.
3	$\overline{I2}$	In	Receives signal A11 from CPU. When LOW, Music LSI descriminates data bus input as data.
4	$\overline{CS}$	In	Chip enable terminal. When LOW, the LSI is able to communicate with CPU.
5 ~ 12	D0 ~ D7	In	Data bus
14 ~ 28	SA4 ~ CMZ	Out	LCD drive signals
29	VDD	–	+5V source
30	CLK	Out	Depends on the voltage level of terminal I3, this terminal functions as input or output of clock pulse. When terminal I3 is LOW, this terminal outputs a half frequency of the clock pulse whereas this terminal becomes clock pulse input when I3 is HIGH. In this model, terminal I3 is connected to GND (LOW).
31, 32	PG2, PG1	In/Out	19 MHz clock pulse input and output
33	GND	–	GND (0V) source
34	I3	In	Connected to GND making terminal CLK (pin 30) a clock pulse output.
42, 43, 46, 48	IO7, I0, O3, O2	Out	4-note polyphonic sound signal outputs. In accordance with CASIO CHORD or SPLIT switches statuses, these terminals output melody lower tone, or chord sounds.
50, 52, 55, 56	O1, O4, IO9, IO10	Out	Regardless of CASIO CHORD or SPLIT switches statuses, these terminals always output 4-note polyphonic melody signals.
63	AO0	Out	Chord VCF envelope control voltage. In accordance with the voltage level of this terminal, VCF envelope of chord or lower tone is varied.
64	AO1	Out	Chord VCF cutoff frequency control voltage. In accordance with the voltage level of this terminal, cutoff frequency of chord or lower tone is varied.
65	AO2	Out	Chord VCF resonance control voltage. The voltage output from this terminal controls chord or lower tone's resonance value in Chord VCF.
66	AO3	Out	Melody VCF resonance control voltage. The voltage output from this terminal controls melody's resonance value in Melody VCF.
67	AO4	Out	Melody VCF cutoff frequency voltage. In accordance with the voltage level of this terminal, cutoff frequency of melody sound is determined.
68	AO5	Out	Melody VCF envelope control voltage. In accordance with the voltage level of this terminal, VCF envelope of a melody sound is varied.
69	AO6	Out	Bass pitch signal
70	AO7	Out	LFO signal for Stereo Chorus circuit. In accordance with selected tone, the terminal outputs 140ms ~ 1.2 seconds triangle waveform for chorus speed.
71	P0	Out	Melody VCF mute signal. When the LSI does not generate melody sounds, this terminal falls to LOW muting the Melody VCF output.
72	P1	Out	Chord VCF mute signal. When the LSI does not generate chord or lower tone, this terminal falls to LOW muting Chord VCF output.
73	P2	Out	Bass mute signal. Upon receipt of bass mute command from the CPU, Music LSI falls this terminal LOW for muting Bass circuit.
74	P3	Out	Chord/Lower tone and bass mute request signal. When the LSI does not generate chord, lower tone or bass signals, it drops this terminal LOW to request CPU a mute command.
75	$\overline{MUT}$	Out	Melody mute request signal. When the LSI does not generate melody signal, it drops this terminal LOW to request CPU melody mute command.
76	GND7	–	Ground source for pins 71 ~ 75
77	BAS	Out	Bass pitch signal.

13. MELODY & CHORD CIRCUITS



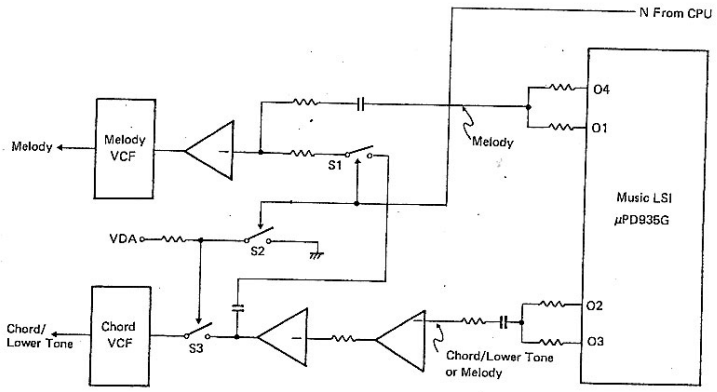
Music LSI μPD935G contains four 7-bit DACs for chord and melody sounds.
Melody Upper DAC generates main melody waveform while Melody Lower DAC produces supplemental waveform and these waveforms are mixed in the ratio of 1:158 as they pass through 820 ohm and 130Kohm resistors.



In order to obtain proper envelope curve, MSB (Most Significant Bit) or inverted MSB signal is added to the waveform.
Upper and Lower Chord DACs generate chord or lower tone sounds when CASIO CHORD or SPLIT is ON and, they produce melody sounds when CASIO CHORD or SPLIT is OFF.
Since each DAC is 4-note polyphonic, eight notes melody sounds can be created when CASIO CHORD or SPLIT is OFF and if one of These switches are ON, Music LSI creates four notes melody and four notes chord or lower tone sounds.

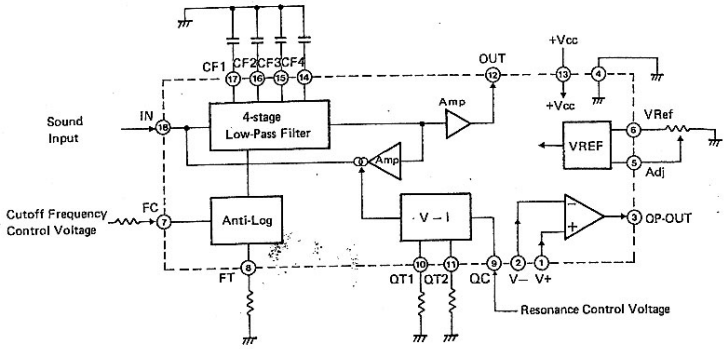
14. MELODY/CHORD CHANGEOVER CIRCUIT

Since Music LSI's O2 and O3 outputs provide either chord/lower tone or melody sounds, this circuit switches the sound signal either to Melody VCF or to Chord VCF depends on the statuses of CASIO CHORD or SPLIT switches.



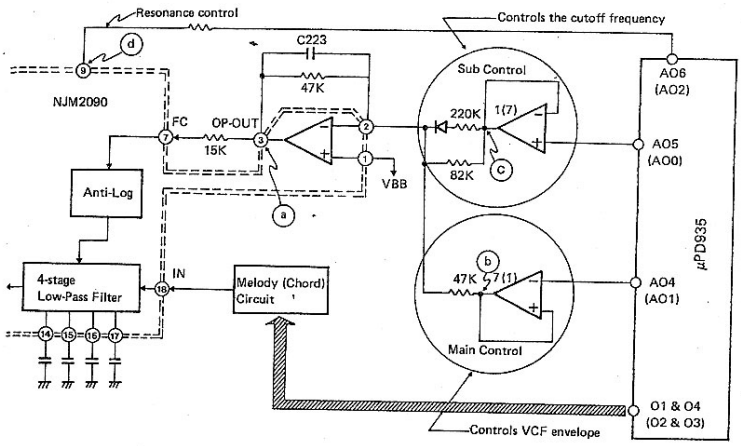
When either CASIO CHORD or SPLIT switches is OFF, the CPU raises signal N turning switches S1, S2 and S3 ON, ON and OFF respectively. Melody signal provided from Music LSI's O2 and O3 terminals enters Melody VCF.
If CASIO CHORD or SPLIT switches is ON, signal N falls to LOW level causing S1, S2 and S3 OFF, OFF and ON so that chord or lower tone output from O2 and O3 passes through Chord VCF.

15. VCF (NJM2090)



NJM2090 is a VCF (Voltage Controlled Filter) which contains 4-stage low-pass filter. Cutoff frequency of the filter is determined by the voltage level of pin 7 (FC). When the voltage is small, cutoff frequency is high and the cutoff frequency reduces if voltage of pin 7 increases. Resonance of the filter varies by the voltage level of pin 9 (QC). The resonance effect is in direct proportion to the voltage level of pin 9, namely, higher the pin 9 voltage, the more effective the resonance.

16. VCF CONTROL CIRCUIT



VCF's cutoff frequency is controlled by the voltage levels of AO5 (AO0 for chord and lower tone) and AO4 (AO1 for chord and lower tone).
In accordance with the set data of VCF parameters (MODE no. 10 ~ 16 for melody, 40 ~ 46 for chord/lower tone), μPD935G's built-in ADCs output voltage levels from terminals AO5 (AO0) and AO4 (AO1).

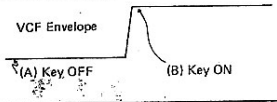
Depends on set data of MODE no. 10, signal AO5 (AO0 for chord/lower tone) varies from 0.8V to 2.5V and controls the VCF cutoff frequency.
Varing its voltage level between 0.5V and 3.5V, AO4 (AO1) controls VCF envelope (MODE no. 12 ~ 16 for melody, 42 ~ 46 for chord/lower tone).

The following table shows the voltage levels at each checkpoints in each MODE and DATA.

(1) Cutoff Control Voltages at MODE 16 (ENVELOPE DEPTH) DATA 0

MODE 10 DATA Value	ⓐ voltage	ⓑ voltage
0	2.5V	0.8V
15	1.7V	1.7V
31	0.8V	2.6V

(2) Cutoff Frequency Control Voltages at MODE 14 (SUSTAIN LEVEL) DATA 31 and MODE 16 (ENVELOPE DEPTH) DATA 31



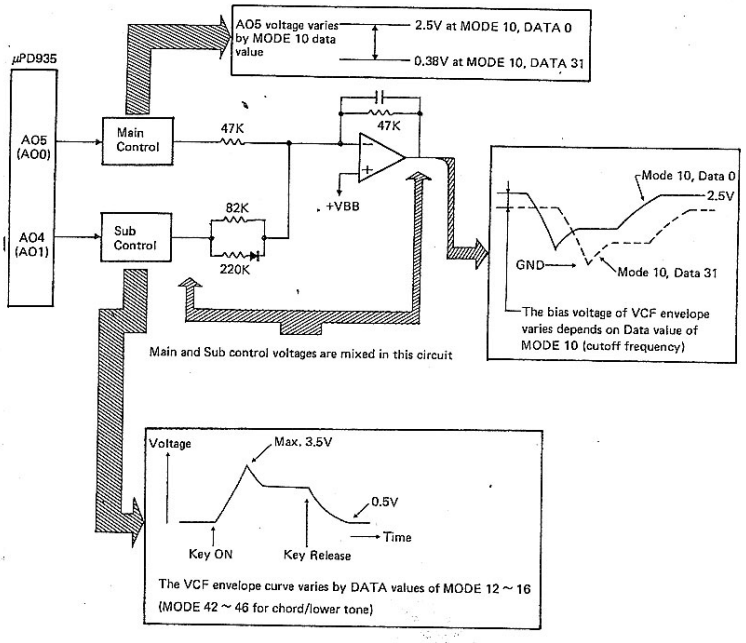
MODE 10 DATA Value		ⓐ voltage	ⓑ voltage	ⓒ voltage
0	(A) Key OFF	2.5V	0.8V	0.5V
	(B) Key ON	0.4V	0.8V	3.6V
15	(A) Key OFF	1.7V	1.7V	0.5V
	(B) Key ON	0.02V	1.7V	3.6V
31	(A) Key OFF	0.8V	2.6V	0.5V
	(B) Key ON	0.02V	2.6V	3.6V

(3) Cutoff Frequency Control Voltages at MODE 14 (SUSTAIN LEVEL) DATA 31, MODE 16 (ENVELOPE DEPTH) DATA 15

MODE 10 DATA Value		ⓐ voltage	ⓑ voltage	ⓒ voltage
0	(A) Key OFF	2.5V	0.8V	0.5V
	(B) Key ON	2.2V	0.8V	1.1V
15	(A) Key OFF	1.7V	1.7V	0.5V
	(B) Key ON	1.4V	1.7V	1.1V
31	(A) Key OFF	0.8V	2.6V	0.5V
	(B) Key ON	0.4V	2.6V	1.1V

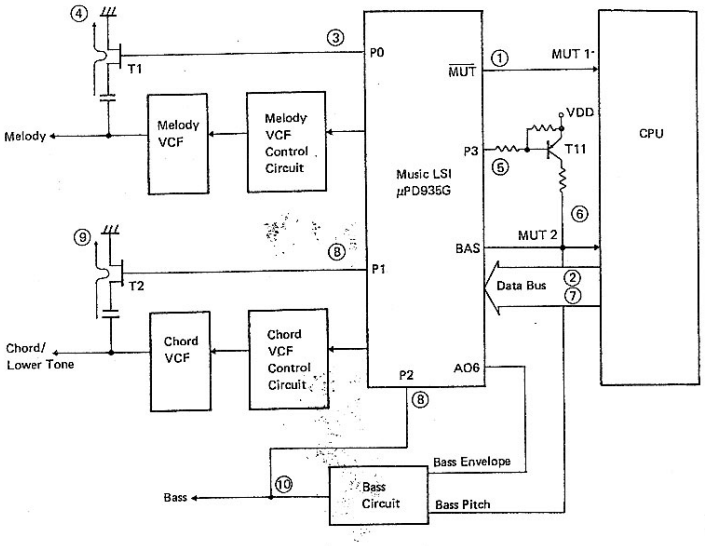
(4) Resonance Control Voltage

MODE 11 DATA Value	ⓓ voltage
0	0.5V
4	1.8V
7	2.2V



17. MUTE CIRCUIT

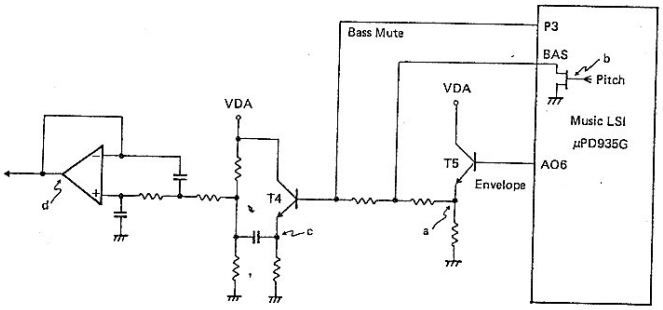
Mute Circuit eliminates noises when the keyboard does not create sounds.



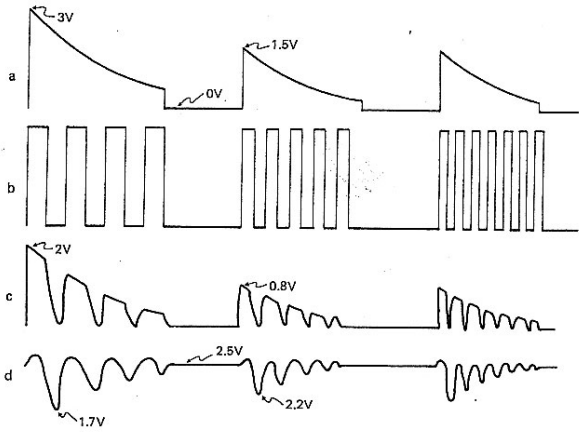
① When Music LSI does not generate melody sounds, it falls signal $\overline{\text{MUT}}$ LOW.
② CPU then sends melody mute command via the data bus.
③ Upon receipt of the command, Music LSI falls signal P0 to turn FET T1 on.
④ Noises which may output from Melody VCF is drained to the gorund.
⑤ If Music LSI does not create chord and bass, it falls signal P3.
⑥ Transistor T11 turns on sending MUT 2 signal to CPU.
⑦ CPU transmits chord/bass mute command through the data bus.
⑧ Music LSI falls signals P1 and P2.
⑨ FET T2 turns on cutting Chord VCF noises.
⑩ By the signal P2, Bass Circuit noises are eliminated.

18. BASS CIRCUIT

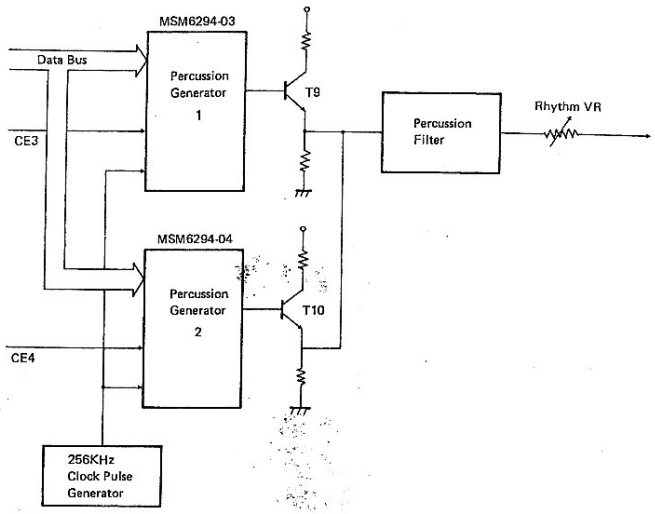
Bass sounds are generated by mixing envelope and pitch waveforms.



Envelope waveform is generated in a Music LSI's built-in DAC and output from terminal AO6.
Transistor T5 amplifies the current of the envelope waveform.
As terminal BAS outputs pitch signals, the pitch and the envelope signals are mixed in transistor T4.
When Music LSI does not generate bass sounds, it falls terminal P3 to eliminate noises.



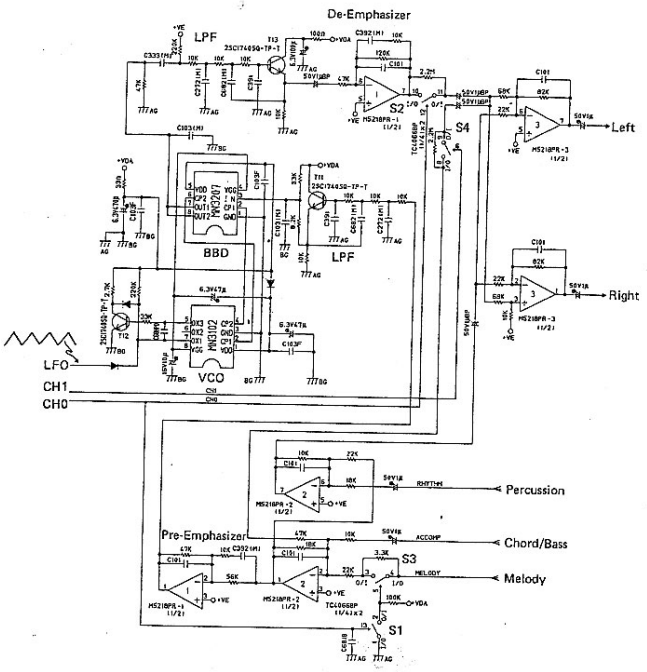
19. PERCUSSION CIRCUIT



Upon receipt of data from the CPU, the Percussion Generators output the following percussion sounds.

Percussion Generator 1 MSM6294-03	Percussion Generator 2 MSM6294-04
Bass Drum, Snare Drum, High-Hat (Open, Closed), Ride Cymbal, Rim Shot, Hand Clap	Synth. Tom (Low, High), A Gogo Bell (Low, High), Conga (Low, High)

20. STEREO CHORUS CIRCUIT

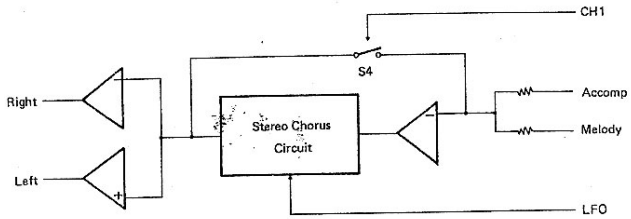


Refer to "BEGINNER'S GUIDE TO CASIOTONE" for Stereo Chorus Circuit Operations. By signals CH0 and CH1 from the CPU, four different stereo chorus effect is given to the preset sounds.

MODE 60 DATA Value	Stereo Chorus Effect	CH0	CH1	LFO Speed
0	OFF	LOW	LOW	–
1	Slow and shallow	HIGH	LOW	1.2 sec.
2	Slow and deep	HIGH	HIGH	0.7 sec.
3	Fast and shallow	HIGH	LOW	140ms

Signal CH0 is provided from the CPU. When DATA value in MODE 60 is "0", the signal falls to LOW causing switches S1, S2, and S3 to turn OFF, OFF and ON respectively for sending melody signal to the Mixer directly and cutting the BBD output.
When DATA value is 1, 2 or 3, signal CH0 rises turning switches S1, S2 and S3 ON, ON and OFF respectively. Melody signal is sent to the right and left channels mixers via Stereo Chorus Circuit.

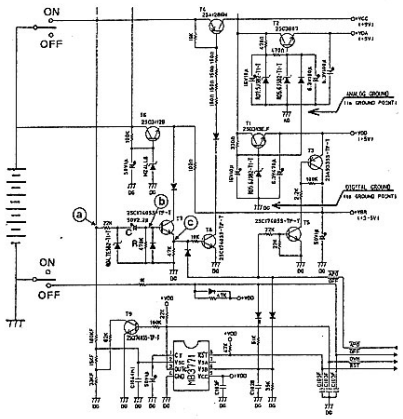
Signal CH1 controls the stereo depth. When MODE 60's DATA value is "2", signal CH1 turns switch S4 ON. Stereo Chorus Circuit output signal is fed-back to the BBD again to deepen the stereo effect.



Chorus speed is controlled by triangle waveform LFO from Music LSI's built-in DAC.

MODE 60 DATA Value	LFO Waveform (Checkpoint: T7 Emitter on PCB MA1M)
0	1.5V
1	3V, 1.2 sec.
2	0.7 sec., 3V
3	140ms, 2V

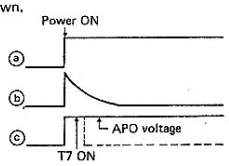
21. POWER CIRCUIT



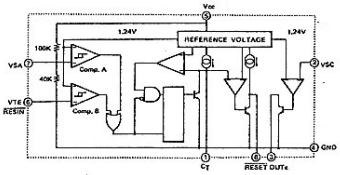
Normally, signal APO from the CPU stays HIGH level turning transistors T8 and T4 on. T4 provides +VCC (+9V) to Power Amplifier. +VCC is also sent to transistors T2 and T1 to make +VDA (+5V for the linear circuits) and +VDD (+5V for the digital circuits).
+VBR (RAM's back up voltage) is generated from +VDD via transistor T3 at Power ON and T6 provides the voltage at Power OFF.

After six minutes from the last operation of the keyboard, the CPU falls signal APO (Auto Power Off), transistors T8 and T4 are turned off to shut all the voltages except +VBR down.

Forming a differential circuit, capacitor C and resistor R turn T7 on for a moment to turn T8 on compulsorily at the first stage of the Power ON.

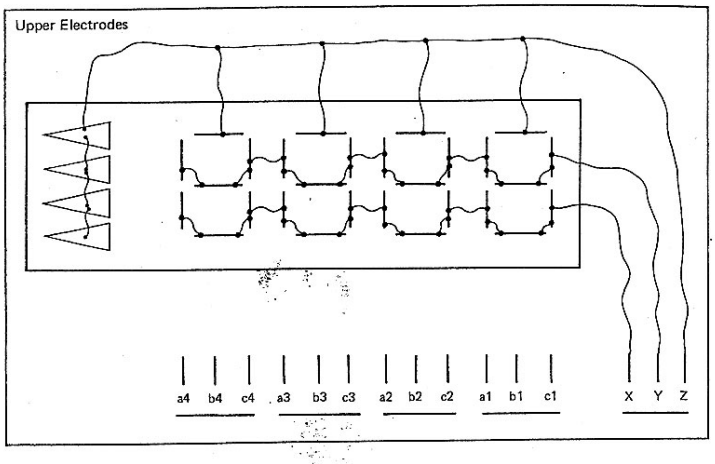


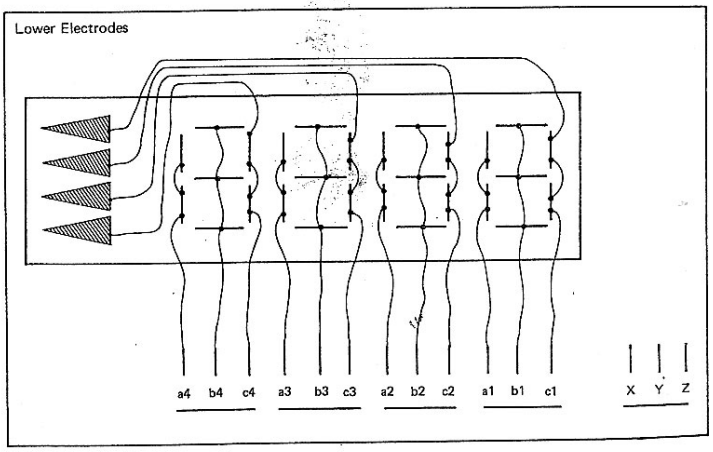
IC MB3771 generates RESET signal and observes the voltage level of the power source.
When the power switch is turned on, MB3771 outputs a LOW level signal from pin 8 to initialize the LSI's internal circuits.
Containing a comparator, MB3771 also observes the battery voltage from pin 2 and if the battery voltage becomes less than six volts, the IC falls pin 3 LOW informing the CPU of the power down. Receiving DWN signal, CPU then flashes the pilot lamp and outputs signal APO six minutes after then to shut the voltages down.



MB3771 Block Diagram

22. LCD WIRING





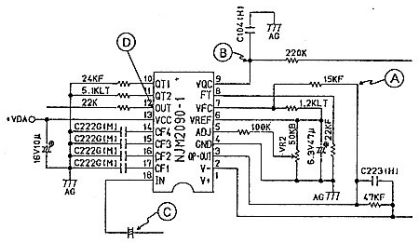
23. ADJUSTMENT

Refer to page 7 for the actual test points.

-1. VCF Cutoff Frequency Adjustment

(1) Ground the points Ⓐ and Ⓑ by means of connecting wires between those points and the ground.

(2) Connect a signal generator to point Ⓒ and send 0.8 Vrms ± 1%, 590 Hz ± 1% signal.



(3) Using a level meter, make sure that the voltage of point Ⓓ is within 0.8V ± 6%.

(4) Adjust the signal generator output level so that the point Ⓓ voltage is within 0.8V ± 2%.

(5) Apply 2.0V ± 1% voltage to point Ⓐ from a voltage regulator.

(6) Adjust VR2 (for melody VCF. For Chord VCF; VR4) so that the voltage of Ⓓ is 0.2 Vrms ± 5%.

(7) Reduce the signal generator output to 0 Vrms and make sure that Ⓓ voltage is between 1.8V and 2.3V.

(8) Perform the same procedures on Chord VCF (Test points Ⓐ′ ~ Ⓓ′.)

-2. VCF Bias Voltage

(1) Set the ENTRY DIAL in MODE "10" (Melody VCF Cutoff Frequency), DATA "0".

(2) Connecting a voltmeter to pin 3 of NJM2090-1, adjust VR5 so that the voltmeter reading is 2.5V ± 20mV.

(3) Setting ENTRY DIAL in MODE "10", DATA "31", make sure that the voltmeter shows 0.8V ± 20mV.

24. TROUBLESHOOTING

Trouble	Faulty Block	Checkpoint
No Power	Power Circuit	Refer to page 3 for check-points' voltage levels.
	MB3771 on PCB MA2M	
	Transistor T4 on PCB MA2M	
	CPU	Make sure that μPD78C10's pin 24 is HIGH during Power ON.
No sound at all	CPU (μPD78C10)	
	ROM (μPD23C256EAC39.40)	
	RAM (HM6264ALSP-15)	
	Address Latch (TC74HC373)	
	Oscillator 1	Waveform ⑮
	Power Circuit	Check the voltages +VCC (+9V), +VDD (+5V), and +VDA (+5V).
One of the speakers does not sound	Opamp M5218PR-3 on PCB MA2M	Pins 1 and 7 of the opamp
	Power Amp LA4127-1 (Right) or LA4127-2 (Left)	Pin 17 of Power Amps
	Speaker	
No Filter Effect	Melody VCF (NJM2090-1) or Chord VCF (NJM2090-2)	Waveforms ①~⑧
	Melody (or Chord) VCF Control Circuit	Pins 1 and 7 of LA6358-2 (for melody) and LA6358-3 (for chord)
	Music LSI (μPD935G)	Voltage levels of Music LSI's pins 63, 64, 67 and 68
No melody, chord or bass sound	Music LSI (μPD935G)	Waveforms of pins 46, 48 (chord), 50, 52 (chord), and 69, 77 (bass)
	Oscillator 2	
	CPU (μPD78C10)	

No percussions	Percussion Generator 1 (MSM6294-03) or Percussion Generator 2 (MSM6294-04)	Waveforms ⑨ and ⑩
	Percussion Filter	Waveform of T8 Emitter
	Oscillator 3	
	RHYTHM volume VR	
	CPU (μPD78C10)	
LCD does not indicate properly	Melody LSI	μPD935G pins 14 ~ 28
	LCD	
	Heat seal	
	Transistors T1 ~ T14	
No key entry at all	Key Input Buffer (TC74HC368P)	
	Decoder (TC74HC139P)	
	Chip Selector (TC74HC138P)	
No switch entry at all	Switch Input Buffer (TC74HC368P on PCB MA4M)	
	Decoder (TC74HC139P)	
	CPU (μPD78C10)	
Certain keys or switches do not function	Open circuit of KC, KI or SI lines	
	Dirty contacts.	
	Key input Buffer (TC74HC368P on PCB MA1M) or Switch Input Buffer (TC74HC368P on PCB MA4M)	
No RAM Card Access	RAM Card	
	Address Latches (TC74HC174P and TC74HC374P)	
	RAM Card connector	
	CPU (μPD78C10)	
	ROM (μPD23C256EAC-39.40)	
	RAM (HM6264ALSP-15)	